



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,649	03/29/2001	Hongjiang Song	INTL-0550-US (P11109)	5728
7590 11/26/2004			EXAMINER WARE, CICELY Q	
Timothy N. Trop TROP, PRUNER & HU, P.C. STE 100 8554 KATY FWY HOUSTON, TX 77024-1805			ART UNIT 2634	
DATE MAILED: 11/26/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

<p align="center"><b>Office Action Summary</b></p>	<b>Application No.</b> 09/821,649	<b>Applicant(s)</b> SONG, HONGJIANG	
	<b>Examiner</b> Cicely Ware	<b>Art Unit</b> 2634	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 July 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6, 8-14, 16-21 and 23 is/are rejected.
- 7) ☒ Claim(s) 7, 15 and 22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

- |    |  |    |        |
|----|--|----|--------|
| 1. | Application/Control Number: 09/821,649 | 2. | Page 2 |
| 3. | Art Unit: 2634                         | 4. |        |
| 5. |  |    |        |

### DETAILED ACTION

1. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

#### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 1, 2, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by O'Connor et al. (US Patent 6,456,676).

(1) With regard to claim 1, O'Conner et al. discloses in (Fig. 3 (360-364)) a locked loop circuit; and a processor (Fig. 2 (210-218, 220)) coupled to the locked loop circuit (Fig. 2 (230, 250, 260), Fig. 3 (230, 262, 362)) to control the locked loop circuit and perform at least one other function (Fig. 2 (235)) in the system not related to the control of the locked loop circuit (col. 3, lines 11-13, 16-19).

- |    |  |    |        |
|----|--|----|--------|
| 1. | Application/Control Number: 09/821,649 | 2. | Page 3 |
| 3. | Art Unit: 2634                         | 4. |        |
| 5. |  |    |        |

(2) With regard to claim 2, claim 2 inherits all the limitations of claim 1. O'Connor et al. further discloses in (Fig. 3) wherein the locked loop circuit comprises a delay locked loop circuit (360-364) (col. 3, lines 11-13, 16-19).

(3) With regard to claim 16, claim 16 inherits all the limitations of claim 1.

(4) With regard to claim 17, claim 17 inherits all the limitations of claims 16 and 2 above.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3-6, 8-14, 18-21 and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor et al. (US Patent 6,456,676) as applied to claim 1, in view of Silvestri (US Patent Application 2002/0130691 A1).

(1) With regard to claim 3, claim 3 inherits all the limitations of claim 1. However O'Connor et al. does not disclose wherein the locked loop circuit comprises: an interface accessible by the processor.

However Silvestri discloses in (Fig. 1, Fig. 2) wherein the locked loop circuit (Fig. 1 (26)) comprises: an interface accessible by the processor (Fig. 2 (12, 34, 54)).

1. Application/Control Number: 09/821,649

2. Page 4

3. Art Unit: 2634

4.

5.

(2) With regard to claim 4, claim 4 inherits all the limitations of claim 3. Silvestri further discloses (Fig. 2 (54)) wherein the interface indicates a phase difference between an input clock signal and an output clock signal generated by the locked loop circuit (Fig. 3, pg. 3, col. 2, lines 22-49).

(3) With regard to claim 5, claim 5 inherits all the limitations of claim 3. Silvestri further discloses in (Fig. 1) wherein the system comprises a computer system (26) having a system memory (Fig. 2 (38)) and the interface (Fig. 2 (12)) is addressable (Fig. 2 (34)) in a range of addresses used to access the system memory (Pg. 2, col. 2, lines 5-24, pg. 3, col. 1, lines 6-41).

(4) With regard to claim 6, claim 6 inherits all the limitations of claim 3. Silvestri further discloses in (Fig. 2 (54, 12), Fig. 3 (62)) wherein the interface indicates storage accessible by the processor to store an indication of a delay used by the locked loop circuit (Pg. 3, col. 2, lines 51-67).

(5) With regard to claim 8, claim 8 inherits all the limitations of claim 1. Silvestri further discloses in (Fig. 1 (12), Fig. 2 (12)) wherein the processor comprises a microprocessor (Pg. 2, col. 1, lines 34-41).

(6) With regard to claim 9, claim 9 inherits all the limitations of claim 1. Silvestri further discloses a system memory storing a program, wherein the processor executes the program to perform said other function (Pg. 2, col. 2, lines 5-24).

(7) With regard to claim 10, O'Connor further discloses in (Fig. 3) an interface accessible by a processor (Fig. 2 (210-218, 220)) to control the locked loop circuit (Fig.

3 (360-364)) to adjust a timing between the input clock signal and the output clock signal (col. 5, lines 19-38).

(8) With regard to claim 11, claim 11 inherits all the limitations of claims 10 and 2 above.

(9) With regard to claim 12, claim 12 inherits all the limitations of claim 10. Silvestri further discloses wherein the interface indicates a phase difference between an incoming clock signal to the locked loop circuit and another signal generated by the locked loop circuit (Pg. 3, col. 2, lines 22-49).

(10) With regard to claim 13, claim 13 inherits all the limitations of claims 10 and 5 above.

(11) With regard to claim 14, claim 14 inherits all the limitations of claim 10. Silvestri further discloses wherein the interface includes storage accessible by the processor to store an indication of a delay applied by the locked loop circuit to the input clock signal (Fig. 2 (54, 12), Fig. 3 (56, 58)).

(12) With regard to claim 18, claim 18 inherits all the limitations of claim 16. Silvestri further discloses in (Fig. 2 (30)) performing at least one of read and write operations to the interface to control the locked loop circuit (Pg. 3, col. 1, lines 51-61, col. 2, lines 10-20).

(13) With regard to claim 19, claim 19 inherits all the limitations of claims 16 and 4 above.

1. Application/Control Number: 09/821,649

2. Page 6

3. Art Unit: 2634

4.

5.

(14) With regard to claim 20, claim 20 inherits all the limitations of claims 16 and 5 above.

(15) With regard to claim 21, claim 21 inherits all the limitations of claims 16 and 6 above.

(16) With regard to claim 23, claim 23 inherits all the limitations of claims 16 and 8 above.

#### ***Allowable Subject Matter***

6. Claims 7, 15 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: The instant application discloses a system comprising a locked loop circuit and a processor coupled to the locked loop circuit to control the locked loop circuit and perform at least one other function in the system not related to the control of the locked loop circuit. Prior art references show similar methods but fail to teach; **“wherein the interface includes storage accessible by the processor to store an indication of a selection of one or more of a plurality of output clock signals furnished by the locked loop circuit”**, as in claims 7, 15, 22.

- |    |  |    |        |
|----|--|----|--------|
| 1. | Application/Control Number: 09/821,649 | 2. | Page 7 |
| 3. | Art Unit: 2634                         | 4. |        |
| 5. |  |    |        |

**Conclusion**

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cicely Ware whose telephone number is 703-305-8326. The examiner can normally be reached on Monday – Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

*Cicely Ware*

cqw  
November 23, 2004

  
AMANDA T. LE  
PRIMARY EXAMINER